

ABSTRACT

A scheme for Built-in-Self-Test (BIST) of analog signals with minimal area overhead, for measuring on-chip voltages in an all-digital manner is presented in this thesis. With technology scaling, the inverter switching times are becoming shorter thus leading to better resolution of edges in time. This time resolution is observed to be superior to voltage resolution in the face of reducing supply voltage and increasing variations as physical dimensions shrink. In this thesis, a new method of observability of analog signals is proposed, which is digital-friendly and scalable to future deep sub-micron (DSM) processes. The low-bandwidth analog test voltage is captured as the delay between a pair of clock signals. The delay thus setup is measured digitally in accordance with the desired resolution.

Such an approach lends itself easily to distributed manner, where the routing of analog signals over long paths is minimized. A small piece of circuitry, called sampling head (SpH) placed near each test voltage, acts as a transducer converting the test voltage to a delay between a pair of low-frequency clocks. A probe clock and a sampling clock is routed serially to the sampling heads placed at the nodes of analog test voltages. This sampling head, present at each test node consists of a pair of delay cells and a pair of flip-flops, giving rise to as many sub-sampled signal pairs as the number of nodes. To measure a certain analog voltage, the corresponding sub-sampled signal pair is fed to a Delay Measurement Unit (DMU) to measure the skew between this pair. The concept is validated by designing a test chip in UMC 130 nm CMOS process. Sub-mV accuracy for static signals is demonstrated for a measurement time of few milliseconds and ENOB of 5.29 is demonstrated for low bandwidth signals in the absence of sample-and-hold circuitry.

The sampling clock is derived from the probe clock using a PLL and the design equations are worked out for optimal performance. To validate the concept, the duty-cycle of the probe clock, whose ON-time is modulated by a sine wave, is measured by the same DMU. Measurement results from FPGA implementation confirm 9 bits of resolution.